IN THE SPECIFICATION

Amendments to the Specification:

Please replace the paragraph beginning on page 6, line 8, with the following rewritten paragraph:

FIG. 3 shows a cache memory 30 that is one embodiment of the cache 13 of FIGS. 1 and 2. The cache 30 is configured as a 4-way associative cache, and includes a tag unit 31, a data unit 32, an address converter 33, a select circuit 34, an encoder circuit 35, and a multiplexer (MUX) 36. When requesting data from the cache 30, the CPU 11 provides a main memory address ADDR to the cache 30 to concurrently address the tag unit ~~31~~ 21 and the data unit 32. The main memory address ADDR includes a tag address and a cache index. The address converter 33 provides the tag address to the tag unit 21 and the cache index to the data unit 32. The number of bits in the main memory address ADDR corresponds to the number of address locations in memory 16, while the number of bits in the cache index corresponds to the number of cache lines in the data unit 32. For example, where the data unit 32 includes 256k cache lines, the cache index includes 18 bits.

Please replace the paragraph beginning on page 8, line 32, with the following rewritten paragraph:

To process an address request from the CPU 11, the address converter 33 converts the main memory address ADDR into its tag address and cache index. The cache index is used to simultaneously access a selected cache line 38 of each cache block 32(0)-32(3). In response thereto, all cache blocks, including the disabled cache block 32(0), read out their selected cache line to MUX 36. Concurrently, the tag address is provided to each tag array 31(0)-31(3) and compared with tag entries 39 therein to generate corresponding match signals. The logic high way select signals ws_1 to ws_3 provided to AND gates 34(1)-34(3) cause AND gates 34(1)-34(3) to pass match signals from respective tag arrays 31(1)-31(3) to the encoder circuit 35. The low logic way select signal ws_0 provided to AND gate 34(0) forces the output of AND gate 34(0) to logic low, thereby forcing a mismatch condition for tag array 31(0). In response to these gated match signals, the encoder circuit 35 generates SEL to

select the output of the cache block that corresponds to the matching tag address (if any). For example, if the tag address provided by the address converter 33 matches a tag entry 39 in tag array ~~32(1)~~ 31(1), the encoder circuit 35 generates a select signal SEL that selects corresponding cache block 32(1). If there is not a matching tag entry 39 in any of the tag arrays 31(0)-31(3), the encoder circuit 35 disables MUX 36 so that no output data is provided.